THE HONORABLE JAMES L. ROBART

IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF WASHINGTON
AT SEATTLE

MICROSOFT CORPORATION,

Plaintiff,

vs.

MOTOROLA, INC., ET AL.,

Defendants.

MOTOROLA MOBILITY, INC., et al.,

Plaintiffs,

vs.

MICROSOFT CORPORATION,

Defendants.

Case No. C10-1823-JLR

MICROSOFT CORPORATION'S OPENING CLAIM CONSTRUCTION BRIEF

Hearing Date: March 9, 2012 9:00 a.m.

LAW OFFICES
DANIELSON HARRIGAN LEYH & TOLLEFSON LLP
999 THIRD AVENUE, SUITE 4400
SEATTLE, WASHINGTON 98104
TEL, (206) 623-1700 FAX, (206) 623-8717

TABLE OF CONTENTS

LAW OFFICES
DANIELSON HARRIGAN LEYH & TOLLEFSON LLP
999 THIRD AVENUE, SUITE 4400
SEATTLE, WASHINGTON 98104
TEL, (206) 623-1700 FAX, (206) 623-8717

TABLE OF AUTHORITIES

Page(s)

CASES

LAW OFFICES
DANIELSON HARRIGAN LEYH & TOLLEFSON LLP
999 THIRD AVENUE, SUITE 4400
SEATTLE, WASHINGTON 98104
TEL, (206) 623-1700 FAX, (206) 623-8717

STATUTES

LAW OFFICES
DANIELSON HARRIGAN LEYH & TOLLEFSON LLP
999 THIRD AVENUE, SUITE 4400
SEATTLE, WASHINGTON 98104
TEL, (206) 623-1700 FAX, (206) 623-8717

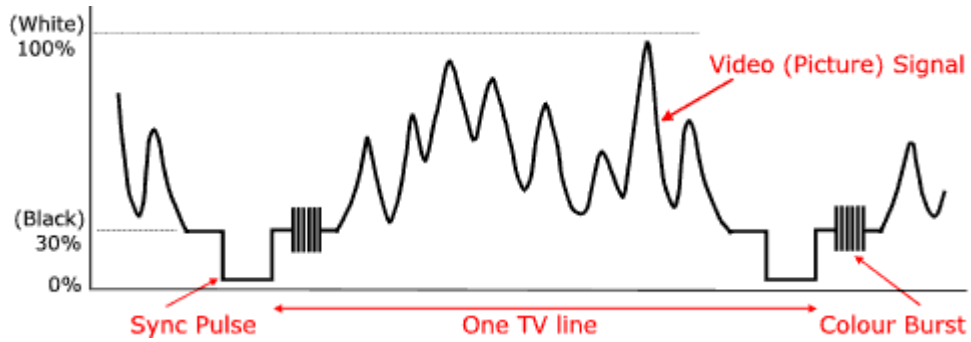
I. INTRODUCTION

Microsoft respectfully submits this opening brief in support of its proposed construction of disputed terms[1] from Motorola Mobility, Inc. ("MMI") U.S. patents 7,310,374, 7,310,375, and 7,310,376 (the "'374," "'375," and "'376" Patents, respectively).[2] These disputed terms potentially affect the alleged infringement and/or invalidity of these patents. The three asserted patents are asserted against the H.264 video coding standard and as such are implicated directly in the RAND issues also pending before the Court.

II. STATEMENT OF THE TECHNOLOGY

General Video Background

These patents relate generally to digital video processing. Historically, home televisions captured and interpreted specially-formatted electromagnetic signals transmitted through the air (and later cable lines) to generate the images on the screen. These video signals historically were analog, meaning that they varied in magnitude and frequency over time based on the output of the television camera. This time variance for one line is illustrated below, along with formatting information to place the image on the screen:

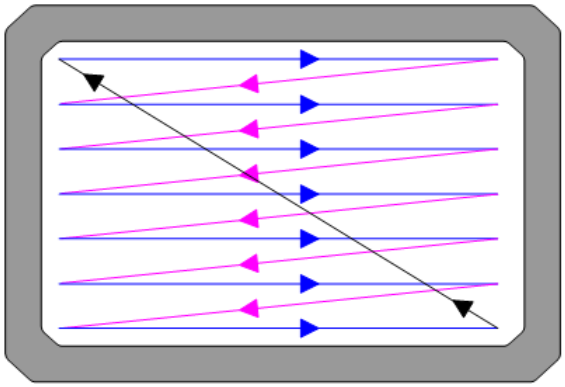


[1] This brief addresses the ten terms jointly identified by the parties on January 27, 2012. Whether additional terms require construction will be determined pursuant to the procedures set forth by the Court during the January 24, 2012 status hearing.

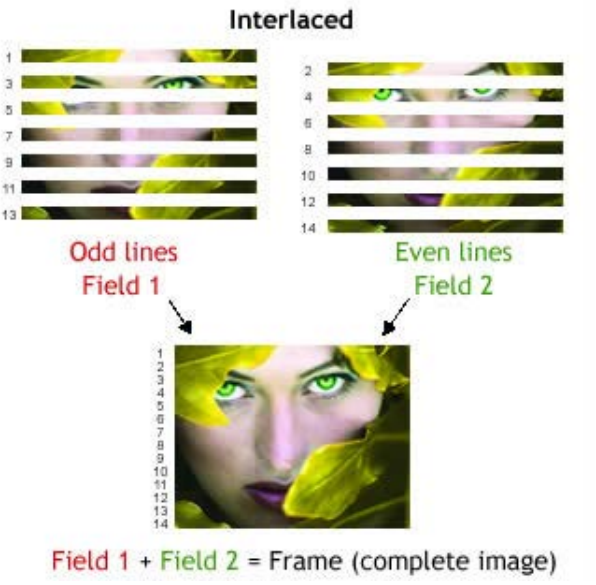
[2] Throughout this brief, Microsoft generally cites only the '374 specification. The '375 and '376 specifications are the same as the '374 specification.

LAW OFFICES
DANIELSON HARRIGAN LEYH & TOLLEFSON LLP
999 THIRD AVENUE, SUITE 4400
SEATTLE, WASHINGTON 98104
TEL, (206) 623-1700 FAX, (206) 623-8717

Analog televisions created visible images by sweeping an electron beam across the back side of the TV picture tube, causing the screen to glow in a pattern representing the desired image. The electron beam traced "lines" across the screen. Every 1/60th of a second, that electron beam would trace each line from left to right on the screen, advancing from top to bottom, as shown below.



To improve resolution on these older systems, television engineers introduced "interlaced" video. Interlaced video doubled the lines shown on the screen by first sending the odd lines on the screen, followed 1/60th of a second later by the even lines. The odd and even lines were interleaved as illustrated below:



LAW OFFICES
DANIELSON HARRIGAN LEYH & TOLLEFSON LLP
999 THIRD AVENUE, SUITE 4400
SEATTLE, WASHINGTON 98104
TEL, (206) 623-1700 FAX, (206) 623-8717

By rapidly changing the images painted on the screen, movement appeared like a motion picture film – that is, by displaying a series of images in sufficiently rapid succession that the human eye perceives a single moving image rather than a "slide show."

Later, technologists recognized that the same video information could be captured digitally, *i.e.*, as "1's" and "0's", transmitted to viewers over the air or cable or provided on a disk like a DVD, and correspondingly reconstructed into a visible video image. Digital processing, however, presented a significant practical hurdle because video requires a massive amount of information. As a result, technologists found ways to compress or otherwise reduce the amount of digital data necessary to reconstruct a video image, using advanced mathematics, statistical predictive algorithms, and human visual characteristics. In the encoding process, some information is often strategically discarded.[3] Corresponding "decoding" techniques were then necessary to reconstruct the original image – more or less – from the encoded information.

Video display technology also has evolved since the early days of electron beams sweeping across the phosphors of a picture tube. Generally, computer and television displays now comprise a rectangular array of picture elements (*i.e.*, "pixels") that can be activated individually. Modern displays form images with each pixel being assigned a value corresponding to its brightness and color. These modern displays do not use interlaced video – *i.e.*, by painting every other line on the screen. Rather, modern displays display content progressively where each line of pixels is painted in order from top to bottom.

Recognizing that videos created using a particular encoding scheme are useless unless consumers have the corresponding technology to decode such video, interested companies in

[3] '374 Patent, at 1:59-67.

LAW OFFICES
DANIELSON HARRIGAN LEYH & TOLLEFSON LLP
999 THIRD AVENUE, SUITE 4400
SEATTLE, WASHINGTON 98104
TEL, (206) 623-1700 FAX, (206) 623-8717

the video technology field have worked together to articulate video standards. In general, companies jointly define the specific characteristics for the standard, thereby enabling interested parties to create content, encoding technology, and decoding technology that interoperate successfully.

Video standards have evolved over time. One widely-adopted standard is known as MPEG-2, which is the format in which standard DVD movies are encoded. As mentioned, MMI has asserted the patents in suit against the H.264 standard, which attempts to improve on MPEG-2 in a number of ways to achieve even greater data compression.

The '374, '375, and '376 Patents Background

MMI's asserted patents relate to the encoding and decoding of digital video information described above but only concern ***interlaced*** digital video content. (*See* '374 Patent, at 1:49-58.) Their common specification describes in detail only the encoding process. The asserted claims, however, also recite decoding that data. (*See* '374 Patent, at 1:62-67.)

As explained, interlaced video images contain two "fields"—one representing the even lines and the other representing the odd lines. ('374 Patent, at cls. 8-18.) Together, two consecutive fields are a "frame." ('374 Patent, at 1:57-58.) Interlaced video can sometimes be better compressed by processing the fields (*i.e.*, even and odd lines) separately (*e.g.*, in motion-filled portions[4]), referred to as "field mode" ('374 Patent, at 7:54-58), and sometimes by processing both fields together (*e.g.*, in relatively motion-free portions), referred to as "frame mode". ('374 Patent, at 7:46-50; '374 Patent, at 4:25-28.) When using this technique, the video encoder described in the patent determines whether *frame* mode or *field* mode is better for a particular portion of video. ('374 Patent, at 4:17-34.) The asserted patents summarize the

[4] "Motion filled" refers to areas of the image with objects moving more rapidly.

LAW OFFICES
DANIELSON HARRIGAN LEYH & TOLLEFSON LLP
999 THIRD AVENUE, SUITE 4400
SEATTLE, WASHINGTON 98104
TEL, (206) 623-1700 FAX, (206) 623-8717

invention as "AFF coding can be performed on smaller portions of a picture. This small portion can be a macroblock, a pair of macroblocks, or a group of macroblocks. Each macroblock, pair of macroblocks, or group of macroblocks or slice is encoded in frame mode or in field mode, regardless of how the other macroblocks in the picture are encoded." ('374 Patent, at 6:57-63.) Figure 7 in the '374 Patent illustrates how the screen is divided into rectangular portions called "macroblocks" and processed in "smaller portions" larger than one macroblock:

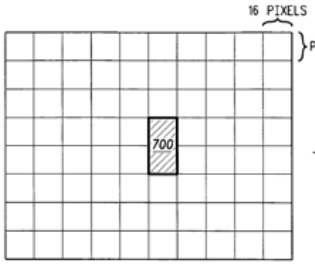


FIG. 7

III. TERMS FOR CLAIM CONSTRUCTION

1. **"macroblock"** '374 Patent, claims 8, 14; '375 Patent, claims 6, 13, 17; '376 Patent, claims 14, 15, 18-20, 22, 23, 26-28, 30. The Parties' Joint Claim Construction Chart (Dkt. 171) at 1-4 ("Joint Claim Chart") (claim element 1 in Joint Claim Chart).

Term	Microsoft's Construction	MMI's Construction
"macroblock"	a rectangular group of pixels	a picture portion comprising a 16×16 pixel region of luma and corresponding chroma samples

Microsoft's construction for "macroblock" tracks the definition in the specification, which expressly defines "macroblock" as "a rectangular group of pixels." ('374 Patent, at 5:56-58.) Because the inventors defined the term "macroblock," their definition should be adopted. *See Phillips v. AWH Corp.*, 415 F.3d 1303, 1316 (Fed. Cir. 2005) (*en banc*).

MMI's contrary proposal introduces at least two changes to the express definition of "macroblock": (1) it limits a "macroblock" to the preferred embodiment's size of 16x16 pixels; and (2) it adds the phrase "region of luma and corresponding chroma samples." Both changes from the express definition should be rejected.

LAW OFFICES
DANIELSON HARRIGAN LEYH & TOLLEFSON LLP
999 THIRD AVENUE, SUITE 4400
SEATTLE, WASHINGTON 98104
TEL, (206) 623-1700 FAX, (206) 623-8717

As to the first, the patents do not *require* a macroblock to have 16 rows and 16 columns, stating instead that "the macroblock has M rows of pixels and N columns of pixels." ('374 Patent, at 7:7-8.) Figure 5 depicts this variable representation—with the macroblock labeled as having dimensions M x N, not 16x16. Specific values are a preferred embodiment: "A ***preferable*** value of N and M is 16, making the macroblock (500) a 16 by 16 pixel macroblock." ('374 Patent, at 7:8-10 (emphasis added); *see also* '374 Patent, at 5:57-58. ("a ***preferable*** macroblock (201) size is 16 by 16 pixels") (emphasis added)).

Claims are limited to the preferred embodiment only in specific situations, none of which applies here. *See Silicon Graphics, Inc. v. AT1 Techs., lnc.*, 607 F.3d 784, 792–93 (Fed. Cir. 2010). Claims, such as those in dispute, that are written to cover generic characteristics typically are not limited to any preferred embodiment, especially with respect to specific sizes. *See Conoco, Inc. v. Energy & Envtl. Int'l, L.C.*, 460 F.3d 1349, 1358 (Fed. Cir. 2006); *Edwards Sys. Tech., Inc. v. Digital Control Sys., Inc.*, 99 F. App'x 911, 919 (Fed. Cir. 2004).

MMI's asserted intrinsic evidence also does not support a 16x16 pixel limitation. MMI cites passages that simply identify the preferred embodiment, but do nothing to define "macroblock." MMI similarly relies on a provisional application (Ex. K to the Joint Claim Chart) for the statement that "[e]ach macroblock is 16x16 pixels." But the provisional application makes this statement in reference to a particular example, and the preceding sentence explains that "[t]he ***typical*** macroblock is 16x16 pixels." (Ex. K to the Joint Claim Chart at ¶ 32 (emphasis added)). Similarly, although other provisional applications (Exs. L, M, Joint Claim Chart) refer to a "[macroblock] of 16x16," neither says that 16x16 is the exclusive size.

MMI's other evidence is similarly unavailing. MMI relies upon a draft MPEG-4 Part

LAW OFFICES
DANIELSON HARRIGAN LEYH & TOLLEFSON LLP
999 THIRD AVENUE, SUITE 4400
SEATTLE, WASHINGTON 98104
TEL, (206) 623-1700 FAX, (206) 623-8717

10 AVC/H.264 standard specification (Ex. N to the Joint Claim Chart) that says a macroblock comprises "[t]he 16x16 luma samples and the two corresponding blocks of chroma samples" (Joint Claim Chart at 3), but ignores that the patents expressly say that they are not intended to be limited to that draft standard specification:

> Although this method of AFF encoding is compatible with and will be explained using the MPEG-4 Part 10 AVC/H.264 standard guidelines, it can be modified and used as best serves a particular standard or application.

('374 Patent, at 4:48-51.) Similarly, MMI relies upon a prior art reference (Ex. O to the Joint Claim Chart) with a 16x16 macroblock, but that does not establish that *all* macroblocks must be 16x16.

MMI's extrinsic evidence should be rejected outright because it seeks to alter the express definition in the specification. *See Novartis Pharms. Corp. v. Abbott Labs.*, 375 F.3d 1328, 1335 (Fed. Cir. 2004). Here, the specification is not ambiguous—it expressly defines "macroblock" as Microsoft has proposed. Yet, MMI proposes to vary the express definition of "macroblock" in the patent using documents explaining how specified standards have defined the macroblock for their own purposes (Exs. X-AA, Joint Claim Chart). MMI, however, ignores other extrinsic evidence showing macroblocks of other sizes. (*See* ISO-IEC/JTCl/SC29/WGll MPEG 91/228, Nov. 1991, Ex. A, at 4 (16x8 macroblocks – illustrated as two 8x8 brightness blocks at the same location as two 8x8 color blocks); ISO/IEC JTC1/SC2/WG11 MPEG 91/221, Ex. B, at 3-4 (16x8 macroblocks); U.S. Patent No. 5,878,166 (filed Dec. 26, 1995, issued Mar. 2, 1999), Ex. C, at 10:12-15, 10:37-38 (discussing macroblocks of 8x8, 8x4, 4x4, and 4x2 pixels in size)).

Finally, MMI has no support for adding add the phrases "region of luma and corresponding chroma samples" into this term's construction. The specification defines a

LAW OFFICES
DANIELSON HARRIGAN LEYH & TOLLEFSON LLP
999 THIRD AVENUE, SUITE 4400
SEATTLE, WASHINGTON 98104
TEL, (206) 623-1700 FAX, (206) 623-8717

macroblock as "a rectangular group of pixels," and uses the term "pixels" dozens of times in the context of macroblocks. (*See, e.g.*, '374 Patent, at 5:56-58, 7:7-14, 7:60-64.) In contrast, the patents do not use "luma," "chroma," or "samples" as part of the definition of macroblock.

2. **"decoding at least one of said plurality of smaller portions at a time in frame coding mode and at least one of said plurality of smaller portions at a time in field coding mode"** '374 Patent, claim 8. Joint Claim Chart 56-67 (claim element 8 in Joint Claim Chart).

Term	Microsoft's Construction	MMI's Construction
"decoding at least one of said plurality of smaller portions at a time in frame coding mode and at least one of said plurality of smaller portions at a time in field coding mode"	removing the frame coding mode from more than one macroblock together and removing the field coding mode from more than one macroblock together to obtain at least one of a plurality of decoded smaller portions	decoding more than one macroblock together in frame coding mode and more than one macroblock together in field coding mode

This term describes the purported invention—removing field/frame coding—as part of the overall decoding process. The parties' proposed "decoding" constructions contain two key disputes: (1) whether this term describes decoding the frame or field coding (Microsoft), or entirely decoding the content (MMI); and (2) whether decoding must be performed together on a multiple block basis at a time (Microsoft), or whether decoding may be performed on a block-by-block basis (MMI).

As to the first dispute, "decoding" as claimed means "decoding" or "removing the frame coding mode" and "removing the field coding mode" to obtain decoded smaller portions. Claim 8's preamble describes the overall decoding process, reciting "decoding an encoded picture having a plurality of smaller portions from a bitstream, comprising:". MMI tries to make this specific "decoding" step have the same scope as the preamble.[5] But this claimed "decoding" step is narrower, describing decoding from "field coding mode" and "frame coding mode" to put the lines back in their original order, if necessary. As explained above, encoding

[5] As a comprising claim, the claim need not recite every step necessary to decode an encoded picture. The claim allows for unnamed steps not at issue here.

LAW OFFICES
DANIELSON HARRIGAN LEYH & TOLLEFSON LLP
999 THIRD AVENUE, SUITE 4400
SEATTLE, WASHINGTON 98104
TEL, (206) 623-1700 FAX, (206) 623-8717

by separately processing even and odd lines can provide better compression in some circumstances. The decoding process must put those lines back in order to reconstitute the video images.

MMI's construction sheds little light on how MMI means to apply this term. But MMI is apparently arguing that this step means completely decoding the content. In other words, rather than decoding the "field coding" or "frame coding" recited in the claim term, MMI argues for a complete reversal of all encoding. As explained, the preamble describes a "method of decoding an encoded picture," but this term describes only removing the frame coding and the field coding, not anything else.

As to the second dispute, Microsoft proposes, consistent with the claim language and file history, that entire pairs or groups of "macroblocks," referred to as smaller portions,[6] be decoded "at a time," meaning "together," rather than individually in their component blocks. MMI's proposed construction ignores the reason the "at a time" limitation was added. Conceptually, MMI's proposal may cover separately processing portions within individual macroblocks so long as a pair or group of macroblocks are processed before moving onto the next pair or group.

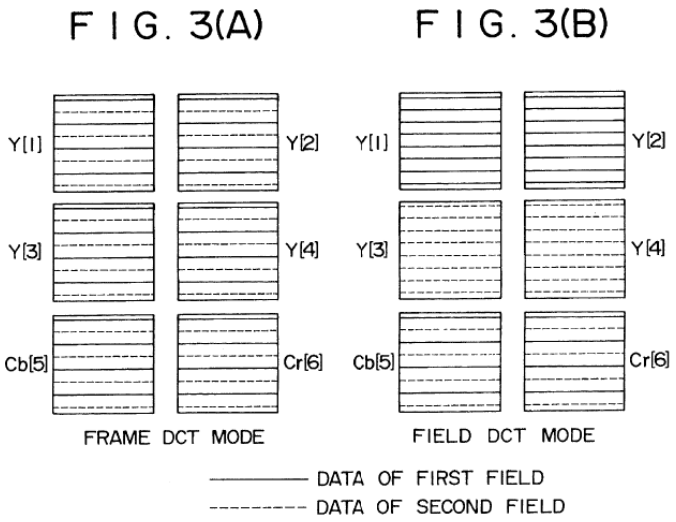
MMI's proposal, however, directly contradicts the basis on which the claims were allowed. The "at a time" language was added to overcome a rejection.[7] During prosecution, the Examiner rejected the claims over a prior art patent, U.S. Patent 5,504,530 (to Obikane et al.). The '530 patent's Figures 3(a) and (b) show the macroblocks broken into numbered blocks (reproduced below), and the '530 patent explains that "within each macro block, the

[6] The claim specifies that "each of said smaller portions has a size that is larger than one macroblock" – *i.e.*, each "smaller portions" is comprised of a pair or larger group of macroblocks.

[7] *See, e.g.,* '374 Patent File History, Reasons for Allowance, June 23, 2007, at 5-6, attached as Ex. D; '374 Patent File History, Examiner's Amendment, June 23, 2007, at 2-4, attached as Ex. E.

LAW OFFICES
DANIELSON HARRIGAN LEYH & TOLLEFSON LLP
999 THIRD AVENUE, SUITE 4400
SEATTLE, WASHINGTON 98104
TEL, (206) 623-1700 FAX, (206) 623-8717

image data is arranged in the 8×8 blocks in raster scanning order. The order in which the blocks Y[1] to Y[4], Cb[5] and Cr[6] are transmitted is indicated by the numbers that are part of the respective symbols." (Ex. F, '530 Patent, at 3:25-30.) The '530 Patent describes performing frame/field coding of macroblocks by processing and "output[ting]" each of these component blocks in sequence. (Ex. F, '530 Patent, at 9:62-10:2.)



That is, Obikane describes processing and outputting macroblocks block-by-block (from 1 to 6), not macroblock-by-macroblock. Because of the Obikane reference, the Examiner added "at a time" to the claims to distinguish block-by-block processing from the issued claim language.

Indeed, the amendment made no changes other than adding "at a time" in three places. Notably, before the amendment, the claims already required acting on two or more macroblocks because the claim already described acting on "smaller portions," and explained that "each of said smaller portions has a size that is larger than one macroblock." ('374 File History, Examiner's Amendment, June 23, 2007, at 2-4, attached as Ex. E.) MMI's construction does not differentiate the final claims from the pre-amended claims and thus would nullify the amendment that the Examiner required for issuance.

Microsoft's construction reflects the Examiner's amendment by requiring the claim to

LAW OFFICES
DANIELSON HARRIGAN LEYH & TOLLEFSON LLP
999 THIRD AVENUE, SUITE 4400
SEATTLE, WASHINGTON 98104
TEL, (206) 623-1700 FAX, (206) 623-8717

process multiple "macroblocks" together and not block by block. The Court should reject MMI's offer to ignore the "at a time" language. A proper claim construction cannot construe the "decoding" function to include precisely what MMI gave up to obtain allowance of the claims. *See Phillips v. AWH Corp.*, 415 F.3d 1303, 1317 (Fed. Cir. 2005) (*en banc*).

3. **"means for decoding at least one of a plurality of processing blocks at a time, each processing block containing a pair of macroblocks or a group of macroblocks, each macroblock containing a plurality of blocks, from said encoded picture that is encoded in frame coding mode and at least one of said plurality of processing blocks at a time that is encoded in field coding mode"** '376 Patent, claim 22. Joint Claim Chart at 11-27 (claim element 3 in Joint Claim Chart).

Term	Microsoft's Construction	MMI's Construction
"**means for decoding at least one of a plurality of processing blocks at a time, each processing block containing a pair of macroblocks or a group of macroblocks, each macroblock containing a plurality of blocks, from said encoded picture that is encoded in frame coding mode and at least one of said plurality of processing blocks at a time that is encoded in field coding mode**"	**Function**: removing the frame coding mode from more than one macroblock together and removing the field coding mode from more than one macroblock together to obtain at least one of a plurality of decoded processing blocks **Structure**: a processor, application specific integrated circuit (ASIC), field programmable gate array (FPGA), coder/decoder (CODEC), or digital signal processor (DSP) performing the algorithm of: in field mode, creating in memory one or more macroblocks each containing one field and one or more macroblocks each containing the other field and processing each such macroblock together with the other macroblocks to create in memory at least two macroblocks containing lines from both fields and in frame mode, creating in memory one or more macroblocks each containing lines from both fields and processing each such macroblock together to create in memory at least two macroblocks containing lines from both fields	This is a means-plus function limitation that must be construed according to 35 U.S.C. §112,¶6 **Function**: decoding at least one of a plurality of processing blocks at a time, each processing block containing a pair of macroblocks or a group of macroblocks, each macroblock containing a plurality of blocks, from said encoded picture that is encoded in frame coding mode and at least one of said plurality of processing blocks at a time that is encoded in field coding mode, wherein said decoding is performed in a horizontal scanning path or a vertical scanning path **Structure**: Decoder, and equivalents thereof

The parties agree that the disputed "means for decoding" term is a means-plus-function limitation that must be construed pursuant to 35 U.S.C. § 112, ¶ 6. In construing a means-plus-function limitation, the Court must identify the function recited for the limitation, and then identify the corresponding structure described in the patent. *Allvoice Computing PLC v.*

LAW OFFICES
DANIELSON HARRIGAN LEYH & TOLLEFSON LLP
999 THIRD AVENUE, SUITE 4400
SEATTLE, WASHINGTON 98104
TEL, (206) 623-1700 FAX, (206) 623-8717

Nuance Comm'ns, 504 F.3d 1236, 1240 (Fed. Cir. 2007). When, as here, the disclosed structure is "a computer, or microprocessor, programmed to carry out an algorithm, the disclosed structure is not the general purpose computer, but rather the special purpose computer programmed to perform the disclosed algorithm." *WMS Gaming, Inc. v. Int'l Game Tech.*, 184 F.3d 1339, 1349 (Fed. Cir. 1999).

The first step is easy here, as the parties agree that the function is recited in the claim language directly after the word "means." *See Creo Prods., Inc. v. Presstek, Inc.*, 305 F.3d 1337, 1344 (Fed. Cir. 2002). The parties, however, dispute the meaning of the identified function. In fact, the parties already seek construction of an analogous "decoding" function in the context of a method step, claim 8 of the '374 Patent, as discussed *supra* Section III(2). The differences in language between the two are not meaningful because "smaller portions" and "processing blocks" have the same meaning. "Smaller portions" are claimed as "ha[ving] a size that is larger than one macroblock." (*See, e.g.*, '374 Patent, at cls. 8, 14; '375 Patent, at cls. 6, 13, 22). "Processing blocks" are claimed as "containing a pair of macroblocks or a group of macroblocks." ('376 Patent, at cls. 22, 30). Because the system does not operate on fractional macroblocks, "larger than one macroblock" (as "smaller portions" is defined) is the same as two or more macroblocks – *i.e.*, "a pair of macroblocks or a group of macroblocks" (as "processing blocks" is defined). The Court should ascribe the same meaning to the "decoding" function in this means element that the Court ascribes to the decoding method step in claim 8 of the '374 patent.

To identify the structure that corresponds to the claimed function, Microsoft's proposal properly tracks the algorithm disclosed in the specification. The Federal Circuit repeatedly has held that "computer-implemented means-plus-function terms [are restricted] to the algorithm

LAW OFFICES
DANIELSON HARRIGAN LEYH & TOLLEFSON LLP
999 THIRD AVENUE, SUITE 4400
SEATTLE, WASHINGTON 98104
TEL, (206) 623-1700 FAX, (206) 623-8717

disclosed in the specification." *Harris Corp. v. Ericsson Inc.*, 417 F.3d 1241, 1253 (Fed. Cir. 2005); *see also WMS Gaming Inc.*, 184 F.3d at 1348. In *Aristocrat Technologies Australia Pty Ltd. v. International Game Technology*, 521 F.3d 1328, 1333 (Fed. Cir. 2008), the Federal Circuit noted that it "has consistently required that the structure disclosed in the specification be more than simply a general purpose computer or microprocessor." The scope of the claim must be limited to "the special purpose computer programmed to perform the disclosed algorithm." *Id.*, quoting *WMS Gaming*, 184 F.3d at 1349; *see also Timeline, Inc. v. Proclarity Corp.*, No. C05-1013JLR, at **3, 5 (W.D. Wash. Apr. 11, 2007) (rejecting proposed structure that was "not limited to an algorithm disclosed in the specification for performing the claimed function"). Indeed, the Federal Circuit recently reaffirmed its *Aristocrat* decision, holding that in identifying the corresponding structure, a patentee could not merely point to "a processor and transceiver alone." *HTC Corp. v. IPCom GmbH & Co.*, No. 2011-1004, slip op. at 17 (Fed. Cir. Jan. 30, 2012). Instead, the patentee "had to identify an algorithm that the processor and transceiver execute"; and the specification "had to do more than parrot the recited function; it had to describe a means for achieving a particular outcome, not merely the outcome itself." *Id.* at 18.

Yet, MMI makes no effort to limit the structure to the algorithm disclosed in the specification. Instead, MMI seeks a construction lacking any structure—a "decoder, and equivalents thereof," which is even more generic than the proposed structures at issue in *Aristocrat* (a "microprocessor . . . [with] appropriate programming") and *WMS Gaming* ("an algorithm executed by a computer"). *See Aristocrat*, 521 F.3d at 1333; *WMS Gaming*, 184 F.3d at 1348; *see also Harris*, 417 F.3d at 1254 ("symbol processor"); *Timeline*, No. C05-1013JLR, at *3 ("main process or main procedure running on a computer and configured to

LAW OFFICES
DANIELSON HARRIGAN LEYH & TOLLEFSON LLP
999 THIRD AVENUE, SUITE 4400
SEATTLE, WASHINGTON 98104
TEL, (206) 623-1700 FAX, (206) 623-8717

call or activate said driver"). Further, MMI's proposal is completely circular as the claimed function is "decoding"; a proper construction must identify how the decoding is performed and what structure performs it.

In contrast, Microsoft properly identifies the disclosed structure and the algorithm disclosed in the specification for performing the claimed function. Indeed, the intrinsic record shows that the disclosed structure is: a processor, application specific integrated circuit (ASIC), field programmable gate array (FPGA), coder/decoder (CODEC), or digital signal processor (DSP) performing the algorithm of: **(a)** *in field mode*, creating in memory one or more macroblocks each containing one field and one or more macroblocks each containing the other field and processing each such macroblock together with the other macroblocks to create in memory at least two macroblocks containing lines from both fields and **(b)** *in frame mode*, creating in memory one or more macroblocks each containing lines from both fields and processing each such macroblock together to create in memory at least two macroblocks containing lines from both fields. ('374 Patent, at Figs. 5, 8; *id.*, at 3:32-33, 6:50-57, 3:50-52, 4:17-34, 6:50-57, 6:58-64; 7:26 – 8:65; *see also* Ex. G.)

4. **"means for decoding at least one of a plurality of smaller portions at a time of the encoded picture that is encoded in frame coding mode and at least one of said plurality of smaller portions at a time of the encoded picture in field coding mode"** '374 Patent, claim 14. Joint Claim Chart at 68-82 (claim element 9 in Joint Claim Chart).

Term	Microsoft's Construction	MMI's Construction
"**means for decoding at least one of a plurality of smaller portions at a time of the encoded picture that is encoded in frame coding mode and at least one of said plurality of smaller portions at a time of the encoded picture in field coding mode, wherein each of said smaller portions has a size that is larger than one macroblock**"	**Function**: removing the frame coding mode from more than one macroblock together and removing the field coding mode from more than one macroblock together to obtain at least one of a plurality of decoded smaller portions **Structure**: a processor, application specific integrated circuit (ASIC), field programmable gate array (FPGA), coder/decoder (CODEC), or digital signal processor (DSP) performing the algorithm of: in field mode, creating in	This is a means-plus function limitation that must be construed according to 35 U.S.C. §112,¶6 **Function**: Decoding at least one of a plurality of smaller portions at a time of the encoded picture that is encoded in frame coding mode and at least one of said plurality of smaller portions at a time of the encoded picture in field coding mode, wherein each of said smaller portions has a size that is larger than one macroblock

LAW OFFICES
DANIELSON HARRIGAN LEYH & TOLLEFSON LLP
999 THIRD AVENUE, SUITE 4400
SEATTLE, WASHINGTON 98104
TEL, (206) 623-1700 FAX, (206) 623-8717

Term	Microsoft's Construction	MMI's Construction
	memory one or more macroblocks each containing one field and one or more macroblocks each containing the other field and processing each such macroblock together with the other macroblocks to create in memory at least two macroblocks containing lines from both fields and in frame mode, creating in memory one or more macroblocks each containing lines from both fields and processing each such macroblock together to create in memory at least two macroblocks containing lines from both fields	**Structure**: Decoder, and equivalents thereof

The parties agree that the disputed "means for decoding" term is a means-plus-function limitation that must be construed pursuant to 35 U.S.C. § 112, ¶ 6. The parties identify functions and structures that are the same as—or as described previously, that have the same meaning as—those proposed for the "means for decoding" element discussed *supra* Section III(3). The same analysis therefore applies here, and Microsoft's proposed construction should be adopted because it sets out the algorithm showing how the decoding function is performed, as set forth in *supra* Section III(3).

5. **"means for selectively decoding at least one of a plurality of smaller portions at a time of the encoded picture that is encoded in frame coding mode and at least one of said plurality of smaller portions at a time of the encoded picture in field coding mode"** '375 Patent, claim 13. Joint Claim Chart at 28-42 (claim element 4 in Joint Claim Chart).

Term	Microsoft's Construction	MMI's Construction
"**means for selectively decoding at least one of a plurality of smaller portions at a time of the encoded picture that is encoded in frame coding mode and at least one of said plurality of smaller portions at a time of the encoded picture in field coding mode**"	**Function**: choosing to remove the frame coding mode from more than one macroblock together or to remove the field coding mode from more than one macroblock together to obtain at least one of a plurality of "decoded smaller portions" **Structure**: a processor, application specific integrated circuit (ASIC), field programmable gate array (FPGA), coder/decoder (CODEC), or digital signal processor (DSP) performing the algorithm of: in field mode, creating in memory one or more macroblocks each containing one field and one or more	This is a means-plus function limitation that must be construed according to 35 U.S.C. §112,¶6 **Function**: selectively decoding at least one of a plurality of smaller portions at a time of the encoded picture that is encoded in frame coding mode and at least one of said plurality of smaller portions at a time of the encoded picture in field coding mode **Structure**: Decoder, and equivalents thereof

LAW OFFICES
DANIELSON HARRIGAN LEYH & TOLLEFSON LLP
999 THIRD AVENUE, SUITE 4400
SEATTLE, WASHINGTON 98104
TEL, (206) 623-1700 FAX, (206) 623-8717

Term	Microsoft's Construction	MMI's Construction
	macroblocks each containing the other field and processing each such macroblock together with the other macroblocks to create in memory at least two macroblocks containing lines from both fields and in frame mode, creating in memory one or more macroblocks each containing lines from both fields and processing each such macroblock together to create in memory at least two macroblocks containing lines from both fields	

The parties agree that the disputed "means for selectively decoding" term is a means-plus-function limitation that must be construed pursuant to 35 U.S.C. § 112, ¶ 6. Furthermore, the parties agree that the function is recited in the claim following the word "means." The parties dispute, however, whether "selectively decoding" requires *choosing* to decode in *either* field mode *or* frame mode (Microsoft), or simply the act of utilizing one mode or the other in the decoding process (MMI).

Claim terms must be construed as written and consistent with their language. Indeed, the claim language itself is the most important evidence for claim construction. *See Phillips*, 415 F.3d at 1312. The very language of this claim term describes a particular action: "***selectively*** decoding . . . in frame coding mode . . . and . . . in field coding mode." (Emphasis added.) Microsoft's construction gives meaning to "selectively," explaining that the claim requires choosing (*i.e.*, *selecting*) the mode in which to decode.

The specification supports Microsoft's construction. Although the specification does not provide any detail about how to select field or frame mode, it explains that:

> The encoder determines which type of coding, frame mode coding or field mode coding, is more advantageous for each picture and chooses that type of encoding for the picture. The exact method of choosing between frame mode and field mode is not critical to the present invention and will not be detailed herein.

LAW OFFICES
DANIELSON HARRIGAN LEYH & TOLLEFSON LLP
999 THIRD AVENUE, SUITE 4400
SEATTLE, WASHINGTON 98104
TEL, (206) 623-1700 FAX, (206) 623-8717

('374 Patent at 4:29-34; *also* 6:50-56.)[8] The proposed innovation of the patent is that it allows selecting between frame mode or field mode on areas smaller than the entire picture. ('374 Patent at 6:57-63.) This focus on active choice is also apparent in claims relating to "encoding" which require "selectively encoding" ('375 Patent, claims 1, 3, 5). The term "selectively," and the choice it represents, should be read consistently among the claims whether that term modifies "encoding" or "decoding."[9] *Omega Eng'g, Inc. v. Raytek Corp.*, 334 F.3d 1314, 1334 (Fed. Cir. 2003). Further, comparing the terms in claims 8 and 14 of the '374 Patent, in which the inventors used the same language disputed here, but without "selectively" modifying "decoding," confirms that "selectively" in claim 13 of the '375 Patent was intended to add a condition. *See Philips*, 415 F.3d at 1314. Only Microsoft's construction gives proper meaning to the term "selectively."

The parties also dispute the structure that corresponds to the claimed "selectively decoding" function. The parties offer the same proposed structures discussed *supra* Sections III(3)-(4) in the context of the "means for decoding" elements. As discussed in those sections, Microsoft's proposal properly tracks the structure and algorithm disclosed in the specification (*See Aristocrat*, 521 F.3d at 1333), whereas MMI's proposal wholly ignores both.

6. **"using said plurality of decoded [smaller portions/processing blocks] to construct a decoded picture"** '374 Patent, claims 8, 14; '375 Patent, claims 6, 13, 17; '376 Patent, claims 14, 22, 30. Joint Claim Chart at 5-10 (claim element 2 in Joint Claim Chart).

Term	Microsoft's Construction	MMI's Construction
"using said plurality of decoded [smaller portions/processing blocks] to construct a decoded picture"	assembling the decoded [smaller portions/processing blocks] to form a decoded "picture"	*No construction necessary.* *If construed:* generating a decoded picture from the plurality of decoded [smaller portions/processing blocks]

[8] Although the claims describe "selecting" in portions smaller than the entire picture, the specification only describes such selecting in the context of picture-level AFF in the locations cited above.

[9] The extrinsic evidence also supports this interpretation, with the first definition for "select" in Webster's New World Dictionary, Second College Edition, being "to choose." (Ex. H).

LAW OFFICES
DANIELSON HARRIGAN LEYH & TOLLEFSON LLP
999 THIRD AVENUE, SUITE 4400
SEATTLE, WASHINGTON 98104
TEL, (206) 623-1700 FAX, (206) 623-8717

Microsoft's proposed construction for the "using" function follows the ordinary meaning of the claim language. The antecedent basis for the "said plurality of decoded [smaller portions or processing blocks]" is the result of the prior "decoding" step, which this step describes using to "construct" a decoded "picture."

As claimed, the "using" step acts on the output of the "decoding" step—specifically, "said plurality of decoded [smaller portions or processing blocks]"— with no intervening processing between these steps.[10] In patent law, "said" refers back to an element previously declared in the claim. *See Energizer Holdings v. International Trade Com'n*, 435 F.3d 1366, 131369-70 (Fed. Cir. 2006). Here, the "said plurality of decoded [smaller portions/processing blocks]" has no possible antecedent basis other than being the unnamed result of the "decoding" step. Construing this term as Microsoft proposes avoids the "antecedent basis problem." *Id.* at 1370-71 (declining to invalidate a claim by finding implicit antecedent basis earlier in the claim).

The specification confirms the plain meaning of the claims. The specification describes assembling or constructing the picture from the decoded smaller portions or processing blocks, labeled 700, like bricks in a wall. (*See, e.g.*, '374 Patent, at Fig. 7.) There is no depiction of any intermediary processing in the figures or, more importantly, in the disputed claim language.

Although MMI contends that no construction is needed for the "using" function, its proposed construction adds a step to the claims. In its construction, MMI adds a "generating" step between the "decoding" and "using" steps. "Generating" some new result which is then

[10] The fact that the claims are "comprising" claims does not change this result. Comprising claims allow other unmentioned steps in addition of the recited steps, but they do not allow adding steps that contravene the language actually in the claims. *See Spectrum Int'l, Inc. v. Sterilite Corp.*, 164 F.3d 1372, 1380 (Fed. Cir. 1998).

LAW OFFICES
DANIELSON HARRIGAN LEYH & TOLLEFSON LLP
999 THIRD AVENUE, SUITE 4400
SEATTLE, WASHINGTON 98104
TEL, (206) 623-1700 FAX, (206) 623-8717

"used", as MMI proposes, simply is not the same as "using "*said* plurality of decoded [smaller portions or processing blocks]." MMI cannot use claim construction to write new claims. *See Resonate Inc. v. Alteon Websystems, Inc.*, 338 F.3d 1360, 1364-65 (Fed. Cir. 2003).

7. **"means for using said plurality of decoded smaller portions to construct a decoded picture"** '374 Patent, claim 14; '375 Patent, claim 13. Joint Claim Chart at 43-47 (claim element 5 in Joint Claim Chart).

Term	Microsoft's Construction	MMI's Construction
"means for using said plurality of decoded smaller portions to construct a decoded picture"	**Function**: assembling the decoded smaller portions to form a decoded "picture" **Structure**: a processor, application specific integrated circuit (ASIC), field programmable gate array (FPGA), coder/decoder (CODEC), or digital signal processor (DSP) performing the algorithm of assembling a decoded picture using the decoded smaller portions like bricks in a wall	This is a means-plus function limitation that must be construed according to 35 U.S.C. §112,¶6 **Function**: using said plurality of decoded smaller portions to construct a decoded picture **Structure**: Decoder, and equivalents thereof

The parties agree that this "means for using" element is in means-plus-function form that must be construed pursuant to 35 U.S.C. § 112, ¶ 6. The parties also agree that the function is recited in the claim language directly after the word "means." The parties dispute, however, the meaning of the identified function. The Court already is construing the identified function, which is identical to the "using" method step, as discussed *supra* Section III(6). Accordingly, the Court should construe the function in the "means for using" element to mean the same as the corresponding function in the method steps.

Microsoft's proposed identification of structure should be adopted for the "means for using" elements for the same legal reasons identified for the "means for decoding" elements, *supra* Sections III(3)-(5). In short, MMI's proposed "structure" ignores well-established Federal Circuit law limiting a means term to the disclosed structure and algorithm. *See, e.g., Aristocrat*, 521 F.3d at 1333. Microsoft's proposal correctly limits the term to the disclosed structure and algorithm, as required by the Federal Circuit. *See id*. Indeed, the specification

LAW OFFICES
DANIELSON HARRIGAN LEYH & TOLLEFSON LLP
999 THIRD AVENUE, SUITE 4400
SEATTLE, WASHINGTON 98104
TEL, (206) 623-1700 FAX, (206) 623-8717

discloses the following: a processor, application specific integrated circuit (ASIC), field programmable gate array (FPGA), coder/decoder (CODEC), or digital signal processor (DSP) performing the algorithm of: assembling a decoded picture using the decoded smaller portions like bricks in a wall. ('374 Patent, at Figs. 5, 7, 8, 9; *id*. at 3:32-33, 3:46-54, 7:43 – 8:45; *see also* Ex. I.) Because Microsoft properly limits the identified structure to the disclosed algorithm, the Court should adopt Microsoft's proposal.

8. **"means for using said plurality of decoded processing blocks to construct a decoded picture"** '376 Patent, claim 22. Joint Claim Chart at 48-52 (claim element 6 in Joint Claim Chart).

Term	Microsoft's Construction	MMI's Construction
"means for using said plurality of decoded processing blocks to construct a decoded picture"	**Function**: assembling the decoded processing blocks to form a decoded "picture" **Structure**: a processor, application specific integrated circuit (ASIC), field programmable gate array (FPGA), coder/decoder (CODEC), or digital signal processor (DSP) performing the algorithm of assembling a decoded picture using the decoded processing blocks like bricks in a wall	This is a means-plus function limitation that must be construed according to 35 U.S.C. §112,¶6 **Function**: using said plurality of decoded processing blocks to construct a decoded picture **Structure**: Decoder, and equivalents thereof

The only difference between the "means for using" elements in this section and in Section III(7) is the use of the words "smaller portions" versus "processing blocks" in describing the function. As discussed previously, the use of "smaller portions" versus "processing blocks" presents a distinction without a difference. *See* Section III(3). Hence, the same analysis set forth *supra* Section III(7) applies here. The same meaning ascribed to the "using" function discussed in Section III(6) should apply to both "means for using" elements. And the same structure and algorithm corresponds to the claimed function. The proper structure is the one identified by Microsoft, which includes the disclosed structure and algorithm. *See supra* Section III(7).

9. **wherein at least one block within [said] at least one of said plurality of smaller portions [at a time] is encoded in inter coding mode** '374 Patent,

LAW OFFICES
DANIELSON HARRIGAN LEYH & TOLLEFSON LLP
999 THIRD AVENUE, SUITE 4400
SEATTLE, WASHINGTON 98104
TEL, (206) 623-1700 FAX, (206) 623-8717

claims 8, 14. Joint Claim Chart at 53-55 (claim element 7 in Joint Claim Chart).

Term	Microsoft's Construction	MMI's Construction
"wherein at least one block within [said] at least one of said plurality of smaller portions [at a time] is encoded in inter coding mode"	encoding at least one block within at least one of said plurality of smaller portions at a time in inter coding mode	wherein at least one block within [said] at least one of said plurality of smaller portions [at a time] is encoded in inter coding mode, a coding mode that uses information from both within the picture and from other pictures

Microsoft construes the "is encoded" term to have the meaning shown by the claims and the specification. MMI just repeats the disputed language and instead defines "inter coding mode." The parties' primary dispute, however, is not over the definition of inter coding mode, but rather whether this element requires the action of encoding "at least one block . . ." or instead refers to the state of being encoded.

The claim language fully supports construing "is encoded" as the act of encoding. Indeed, the claims use a different, more descriptive term to identify the pre-existing state of being encoded: "encoded picture that is encoded." ('374 Patent, at 19:11 (claim 14).) These distinct terms, used in the same claim, should not normally be construed to have the same meaning. *See Primos, Inc. v. Hunter's Specialties, Inc.*, 451 F.3d 841, 848 (Fed. Cir. 2006). Moreover, the claims' use of "at a time" to modify "is encoded" only makes sense if "is encoded" refers to the act of encoding rather than the state of having been encoded.

The dependent claims also support this construction. For example, claim 8 of the '375 patent identifies the input to the encoding process and makes clear that encoding is occurring: "for said current block, said neighboring blocks comprises at least one of a neighboring block that is left of said current block *to be encoded* and a neighboring block that is above said current block *to be encoded*." ('375 Patent, at 18:60-64 (emphasis added).) Other claims have similar language. (*See, e.g.*, '375 Patent, at 19:5-9 (claim 11) ("wherein said most probable prediction mode for a current block is selected in accordance with a neighboring block that is

LAW OFFICES
DANIELSON HARRIGAN LEYH & TOLLEFSON LLP
999 THIRD AVENUE, SUITE 4400
SEATTLE, WASHINGTON 98104
TEL, (206) 623-1700 FAX, (206) 623-8717

left of said current block to be encoded and a neighboring block that is above said current block to be encoded").)

The specification also supports this construction, using the term "is encoded" to signify the act of encoding. For example:

> In intra coding, the macroblock *is encoded* without temporally referring to other macroblocks. On the other hand, in inter coding, temporal prediction with motion compensation is used to code the macroblocks.

('374 Patent, at 9:11-15 (emphasis added); *see also* '374 Patent, at 4:21-28, 5:16-18 & 23-25, 6:57-64 (use of "is encoded" to mean the action of encoding).)

10. **"wherein at least one motion vector is received for said at least one block within at least one of said plurality of smaller portions"** '374 Patent, claims 9, 15. Joint Claim Chart at 83-84 (claim element 10 in Joint Claim Chart).

Term	Microsoft's Construction	MMI's Construction
"wherein at least one motion vector is received for said at least one block within at least one of said plurality of smaller portions"	receiving as part of the bitstream at least one value containing the amount of temporal motion required for the image to move to a new temporal position in the picture for each "said at least one block within at least one of said plurality of smaller portions"	*No construction necessary.* *If construed:* wherein at least one value is received for said at least one block within at least one of said plurality of smaller portions, from which an amount of motion may be determined

The central dispute here is the meaning of "at least one motion vector is received." Microsoft's proposal applies the ordinary meaning of the claim language and requires that the "at least one motion vector" actually be received. MMI, on the other hand, changes the claim language to allow anything to be "received" from which one can then determine "an amount of motion."

The plain language of the claims supports Microsoft's construction:

> 9. The method of claim 8, wherein at least one motion vector is received for said at least one block within at least one of said plurality of smaller portions.

'374 Patent, claim 9. This language describes *receiving* a specific piece of data—"at least one

LAW OFFICES
DANIELSON HARRIGAN LEYH & TOLLEFSON LLP
999 THIRD AVENUE, SUITE 4400
SEATTLE, WASHINGTON 98104
TEL, (206) 623-1700 FAX, (206) 623-8717

motion vector." Microsoft's construction preserves that meaning. The claim does not mention determining the amount of motion; it recites *receiving* a motion vector.

The specification also supports Microsoft's proposal. The '374 Patent expressly says that the encoder can transmit the motion vectors: "The motion vectors (406) used for the temporal prediction with motion compensation need to be encoded and transmitted." ('374 Patent, at 6:29-31.) If the encoder transmits the motion vector, the decoder (the subject of claims 9 and 15) presumably receives the motion vector.

Conversely, MMI's construction improperly conflates "motion vector" with other values from which one can determine motion vectors. MMI relies on the following language in the specification:

> Each block in a frame or field based macroblock can have its own motion vectors. The motion vectors are spatially predictive coded. **According to *an embodiment* of the present invention, in inter coding, prediction motion vectors (PMV) are also calculated for each block.** The algebraic difference between a block's PMVs and its associated motion vectors is then calculated and encoded. This generates the compressed bits for motion vectors.

('374 Patent, at 9:38-45 (emphasis added).) But this excerpt distinguishes between motion vectors ("its associated motion vectors"), and the values used to calculate them (the "algebraic difference" and the "block's PMV"). MMI's construction would allow the "algebraic difference" to be the "motion vector"—but as the patent explains, they are different things. *See Ergo L.L.C. v. Pacific Cycle, Inc.*, No. C09-488JLR, at *6 (W.D. Wash. Sept. 24, 2010) (Markman Order).

Furthermore, other claims in the '374 Patent describe "prediction motion vectors" and their use in "calculat[ing]" the difference. (*See, e.g.*, '374 Patent, claims 12, 13.) Notably, claims 9 and 15 do not include such language and instead describe receiving the motion vector

LAW OFFICES
DANIELSON HARRIGAN LEYH & TOLLEFSON LLP
999 THIRD AVENUE, SUITE 4400
SEATTLE, WASHINGTON 98104
TEL, (206) 623-1700 FAX, (206) 623-8717

fully formed without performing a calculation. Because claims 9 and 15 do not describe "determining" an amount of motion, the inventors clearly intended those claims to have a different meaning. *See Aerotel, Ltd. v. T-Mobile USA, Inc.*, No. C07-1957JLR, at 24 (W.D. Wash. Dec. 23, 2009) (Markman Order) ("In order to give each claim term effect, . . . the court construes the terms differently.") (internal citation omitted), *aff'd, Aerotel, Ltd. v. T-Mobile USA, Inc.*, 2010 WL 5376233 (Fed. Cir. Dec. 20, 2010).

IV. CONCLUSION

For the foregoing reasons, Microsoft requests that its constructions be adopted.

DATED this 3rd day of February, 2012.

DANIELSON HARRIGAN LEYH & TOLLEFSON LLP

By __/s/ Arthur W. Harrigan, Jr._____
Arthur W. Harrigan, Jr., WSBA #1751
Christopher Wion, WSBA #33207
Shane P. Cramer, WSBA #35099

By __/s/ T. Andrew Culbert_____
T. Andrew Culbert, WSBA #35925
David E. Killough, WSBA #40185
MICROSOFT CORPORATION
1 Microsoft Way
Redmond, WA 98052
Phone: 425-882-8080
Fax: 425-869-1327

David T. Pritikin, *Pro Hac Vice*
Richard A. Cederoth, *Pro Hac Vice*
Douglas I. Lewis, *Pro Hac Vice*
John W. McBride, *Pro Hac Vice*
SIDLEY AUSTIN LLP
One South Dearborn
Chicago, IL 60603
Phone: 312-853-7000
Fax: 312-853-7036

LAW OFFICES
DANIELSON HARRIGAN LEYH & TOLLEFSON LLP
999 THIRD AVENUE, SUITE 4400
SEATTLE, WASHINGTON 98104
TEL, (206) 623-1700 FAX, (206) 623-8717

Brian R. Nester, *Pro Hac Vice*
SIDLEY AUSTIN LLP
1501 K Street NW
Washington, DC 20005
Telephone: 202-736-8000
Fax: 202-736-8711

Counsel for Microsoft Corporation

CERTIFICATE OF SERVICE

I hereby certify that on February 3, 2012, I electronically filed the foregoing document with the Clerk of the Court using the CM/ECF system, which will send notification of such filing to the following:

Attorneys for Defendants Motorola Solutions, Inc., Motorola Mobility, Inc., and General Instrument Corporation

Philip S. McCune
Lynn M. Engle
Summit Law Group

Steven Pepe
Jesse J. Jenner
Norman Beamer
Paul M. Schoenhard
Ropes & Gray

/s/ Linda Bledsoe
LINDA BLEDSOE

LAW OFFICES
DANIELSON HARRIGAN LEYH & TOLLEFSON LLP
999 THIRD AVENUE, SUITE 4400
SEATTLE, WASHINGTON 98104
TEL, (206) 623-1700 FAX, (206) 623-8717